



PATENT

IN THE UNITED STATES PATENT OFFICE

Applicant:

David P. Schultz

Assignee:

Xilinx, Inc.

Title:

"Method and System for Flexibly Nesting JTAG TAP
Controllers for FPGA-Based System-On-Chip (SoC)"

Serial No.: 10/086,129

File Date: February 28, 2002

Examiner: Unknown

Art Unit: 2133

Docket No.: X-1069 US

Conf. No.: 2232

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Technology Center 2100

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant brings to the attention of the Examiner the One Hundred Seven (107) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

These references were cited in related U.S. patent applications. This Information Disclosure Statement is being filed under 37 CFR 1.97(b) prior to the receipt of a first office action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,

Justin Liu
Attorney for Applicant
Reg. No. 51,959

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Julie Matthews
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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application / Conf. No.	10/086,129 / 2232
	Filing Date	February 28, 2002
	First Named Inventor	David P. Sch...
	Examiner Name	Unassigned
	Art Unit	2133
	Patent No.	Technology Center 2100
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Attn: Justin Liu		
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Date	January 16, 2004	Charge any additional fees required/credit any overpayment to our Deposit Account Number: 24-0040

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